Low power digital design in Integrated Power Meter IC

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Abstract - This paper considers the low power design aspects of the digital signal processing blocks embedded into three-phase Integrated Power Meter IC. Several optimization techniques were used to implement power efficient design. The techniques mainly rely on clock and data gating.

Keywords – Low-Power Integrated Power Meter

I. INTRODUCTION

Modern power meter devices relays on single chip referred to as integrated power meter (IPM). The designed IPM incorporates all the required functional blocks for three-phase metering, including a precision energy measurement front-end consisting of Sigma Delta AD converters, digital filters, signal processing block, embedded microcontroller, real-time clock, LCD driver and programmable multi-purpose inputs/outputs.

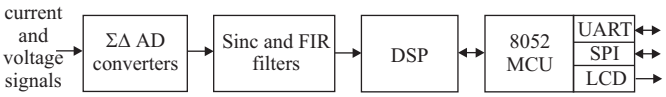

Fig.1 Architecture of the Integrated Power-Meter

The digital filters decimate over-sampled output signals from the on-chip AD converters for both voltage and current signal channels in three phases. The DSP performs the precision computations necessary to measure: active, reactive and apparent energy in four quadrants for all three-phases, instantaneous frequency for each phase, RMS currents and voltages, active, reactive and apparent power and power factor [1].

The microcontroller unit (8052 MCU shown in Fig.1) is compatible with 8052 microprocessors. It includes several communication peripherals: UART, Serial Port Interface (SPI) and LCD driver circuit.

Optimizing power of integrated circuits remains difficult task. This paper considers the low power design aspects of the digital signal processing blocks embedded into three-phase integrated power meter IC.

This paper is organized in five sections and References. The following section gives an overview of power optimization methods applied on DSP block. The third section considers the techniques used for microcontroller's low power optimization. The fourth gives the achieved power consumption for all digital blocks on chip.

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II. LOW POWER TECHNIQUES APPLIED ON DSP BLOCK

A. *DSP's operation*

DSP block receives from filters (through its 16-bit inputs) the digital samples for voltage, current and phase-shifted voltage, and calculates following results: root mean square values for voltage and current, mean values for active and reactive power, apparent power, active and reactive energy, power factor and frequency, [1,2] The measurement results are obtained for all three power line phases. DSP provides three result sets, one set for each power phase. The measurement range for current signal is from 10 mA RMS to 100 A RMS, and up to 300V RMS for voltage. The values are represented by 24-bit numbers.

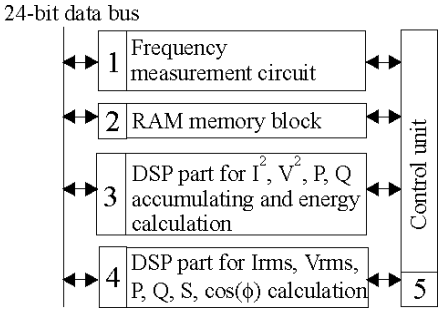

Fig. 2. DSP's block diagram

DSP utilizes controller/datapath architecture and consists of blocks which can be divided into several main groups (Fig. 2):

1. Frequency measurement circuit
2. RAM memory block
3. Part for I^2, V^2, P, Q accumulating and energy calculation
4. Part for current and voltage RMS, active, reactive and apparent power and power factor calculation);
5. Control unit that controls all other parts of DSP.

One of power-line parameters provided by DSP, root-mean-square current - Irms, is calculated once per second. Current samples, obtained from digital filters, are multiplied and the current square values are accumulated over the constant time period of one second. After, derived sum is divided by number of samples, and the root-mean-square current is found after square rooting (according to exp.(1)).

$$Irms = \sqrt{\frac{\sum_{n=1}^{N} i(nT)^2}{N}} \quad (1)$$

The sequence of arithmetical operations for current square summing, performed by Block 3, part of DSP, is shown in Fig.3. The sequence is performed 4096 times per second.

At the sequence beginning, DC offset is removed from instantaneous current values. It is done either by subtracting the constant offset determined during the calibration procedure or by passing the signal through the digital high pass filter. The second doesn't require calibration procedure. After, AC part of instantaneous current is squared in multiplication unit. The value I^2 is passed through the single pole Low Pass Filter (LPF), and after that, it is accumulated into register $AccI^2$ (Fig. 3). All these operations are done by digital circuitry within Block 3. Input (current samples), output (the sum of I^2) and intermediate results (the HPF and LPF registers) are stored outside the Block 3, in one of the three SRAM 64x24 memory blocks. The operations are governed by Control unit - Block 5 in Fig.2.

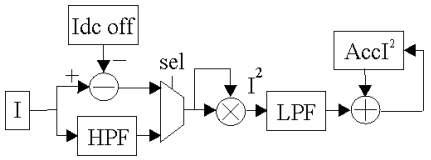

Fig.3. Data processing for current-square accumulation

The same procedure is performed and the same hardware is used for V^2 accumulating. Also, active and reactive power accumulation is done through the same procedure. The only difference is in multiplication process: voltage and current sample-values are used for active power calculation, and current value is multiplied with phase-shifted voltage value to obtain reactive power.

The architecture of Block 3 consists of data registers, arithmetical units for addition and multiplication, and a multiplexer circuit.

After, to generate current root mean square, the intermediate results are passed to Block 4, where, accumulated sum is divided with the constant number 4096 (number of samples). Then, square rooting operation is performed and the result is multiplied with gain correction value, determined during calibration procedure. The same procedure stands for root mean square voltage. The calculation of mean active and reactive power is similar, except there is no rooting. Apparent power is obtained by multiplying root mean square of current and voltage values, and power factor is obtained by dividing active and apparent power values.

Block 4 (Fig. 2) consists of two registers and arithmetical units that implement square rooting, subtraction, multiplication and division. It performs calculations once after every second in the time period which lasts only 1/4096 seconds. The operation time of Block 3, which performs intensive calculations during the one second period, is 4096 times greater then the one of Block4. The power consumption of Block 4 is, therefore, much lower then the power consumed by Block 3.

The chip is implemented in AMI CMOS 0.35um standard cell technology. This technology does not allow low power optimizations at technology and circuit level. CMOS transistors have only single threshold voltage and cells operate at constant 3.3V power supply. The leakage currents can be neglected comparing to dynamic consumption. The power reduction can be achieved at gate and architectural level through the reducing the clock and data switching activity.

The power dissipation of DSP block can be divided into three main areas. The first area is the power cost associated with accesses to the three data memories (represented by Block 2 in Fig.2). The memories power consists of the power consumed within the RAM units themselves, and the power required to transmit the data across the large capacitance of the 24-bit data bus.

Three 64x24 bit memories supplied by technology manufacturer are located near the functional units to minimize the capacitance of the associated wiring. The number of memory accesses of $8*10^5$ gives the power consumption of 150μW.

The second main area of power consumption comes from the energy dissipated in performing the actual operations on the data. This is made of the energy dissipated by transitions within the datapath and clock tree circuitry. In the DSP block, the most of dissipated power comes from Block 3.

The third area is power consumed by control unit block (Block 5 in Fig.2). The control unit is implemented as finite state machine that controls the operations executed within Blocks 3 and 4. It has more than 500 states and occupies significant part of DSP's area.

Comparing to other blocks, Block 3 is active most of time, performs most of calculations, and, communicates with SRAM memories most frequently. It is extracted from design and examined in detail. The sequence of states in Block 5 which controls the operation within Block 3 is also extracted into new design. The used low power techniques that reduce the switching activity are: clock gating, operand isolation, FSM state decomposition and Gray encoding of FSM states. The application of techniques and obtained results are presented onwards in the paper.

B. Clock gating techniques applied to DSP

Clock power is one of the dominant components of total power consumption. The clock signal is fed to most of the circuit blocks and switches every cycle. The clock tree has large capacitances comparing to other nets and reducing the switching activities of clock signal is important.

Clock gating is the technique for dynamic power reduction [5]. It is based on fact that power is saved by

disabling the clock signal to unused circuits. By AND-ing the clock signal with the some gate control signal, clock gating disables the clock to a circuit, avoiding the unnecessary charging and discharging of net capacitances.

The datapath of DSP incorporates several sequential circuits which are not all the time active. For example, arithmetical units for multiplying, dividing and square rooting in DSP are realized as sequential circuits and they have large inactive periods. The unit for multiplication in Block 3 multiplies two operands in 18 clock periods. It is used during chip normal operation four times inside the interval of 256 clock cycles. Therefore, the multiplication unit is inactive during 70% of chip operation time. In Block 4 similar arithmetical units exists: for multiplication, square rooting and dividing. Since those arithmetical blocks are not used all the time, their clock trees can be gated. Only when arithmetical units are active, their clock signals are enabled.

To avoid glitches in clock signal, 2-input AND cell with D latch is used as a gate. The level sensitive D latch holds the input enable signal from the rising edge until the falling edge of the clock. Since the latch captures the state of the enable signal and holds it until the complete clock pulse has been generated, the enable signal needs to be stable around the rising edge of the clock. The signal at the AND cell output is free of glitches and is used as a clock signal of subsequent sequential circuits.

The architecture of Block 3 consists of two 48-bit data registers, arithmetical units for addition and multiplication and a multiplexer circuit. The control unit generates signals for starting the multiplication, selection one of multiplexer's inputs, and, both memory and register data transfer operations. Considering the non-optimized design, the total clock power is a substantial 32% of the circuit's power. The power of non-optimized design is 1104 μW and the power consumed by clock tree is 354 μW. To reduce the clock power, first, the multilplication unit was gated. The design was further power optimized in the way that gating signals are used to write data into registers and memory blocks. The power consumption and area of non-optimized and power optimized design of Block 3 are given in Table I. The power dissipation is improved for 27%. The occupied area remained almost the same as before optimization.

TABLE I

Block	Original design		Optimized by clock gating	
	Area [gates]	Power [μW]	Area [gates]	Power [μW]
Clock tree	8	354	2	89
Registers	456	40	456	32
Three-state circuits	615	106	615	112
Adder	320	143	320	129
Multiplexer	307	48	307	44
Multiplier	663	105	663	96
FSM circuit	990	308	990	303
Total	3359	1104	3353	805

C. Operand isolation low power technique applied to DSP

Operand isolation or data gating reduces power consumption by selectively blocking the unused switching activity caused by redundant propagation of data signals through combinatorial circuits. Data gating is added to high-fanout paths - data buses in the datapath. The bus implementation is usually made of three-state cells. Else, the gating in the datapath main sub-blocks consists of AND gates that stop the propagation of signal to the inputs of unused adders and subtraction circuits.

The multiplexer circuit in Block 3 incorporates multiple parallel data paths. By adding the gating at the multiplexer inputs, the power can be saved. Finaly, three-state buffers were used instead the multiplexer. The 3-8 decoder circuit provides individual enable signals for three-state buffer array. The transparent latch placed in front of decoder is clocked only if its select output is going to change.

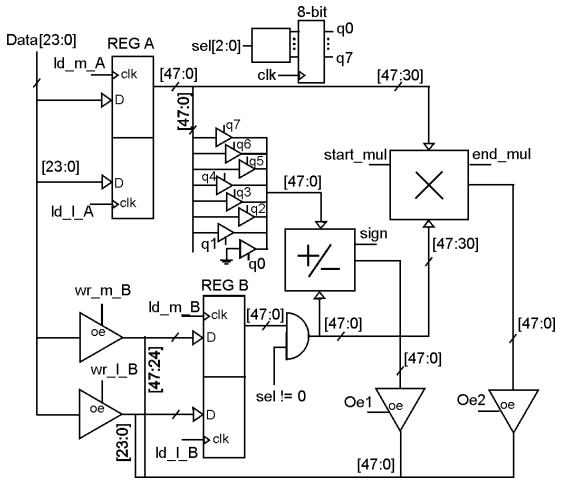

Figure 4 Part for I^2, V^2, P, Q accumulating and energy calculation optimized for low-power by operand isolation and gating

The outputs of three state buffers and register B are connected to the inputs of arithmetical circuit (Fig.4). When control signal which represents the input of 3-8 decoder is in range "001" to "111", the corresponding output enable signal is active and new data pass through three state buffers to the adder input. When "000", the write operation into latch is disabled, and thus, the input of the arithmetical operator is not changed. To isolate the second operand of arithmetical circuit, register B output is gated by AND gating cells. When control signal is in range "001" to "111", data propagation through AND cells is enabled.

The results of optimizations are given in Table II. The modifications in multiplexer circuit didn't give the expected results. The obtained power is increased because of large net capacitances at the three-state circuit outputs.

D. FSM state gray encoding and decomposition

State encoding or state assignment techniques is crucial step in the synthesis of the low-power controller circuitry

[6,7]. The techniques augument the state transition graph with state probabilities, and also, transition probabilities between the states and use these probabilities to guide the state assignment. Adjacent Gray binary encondings are assigned to the states connected with a high probability transition. This minimizes the number of state transitions, thus attempting to minimize switching activity in next state logic and output logic of synthesized FSM.

To consider the impact of state assignment in the consumed power of the combinational part, a number of heuristics are introduced. The key idea of those heuristics is that a combinational circuit optimized in terms of area is also characterized by low-power consumption. Therefore, beside transition probabilities, algorithms take into account the occupied area of the circuit.

The finite state machine that drives the Block 3 controls the operations for removing the DC components from instantanious values of current and voltage signals, else, the generation of current and voltage square, active and reactive power signals and their accumulation over the time, and, generation of pulses necessary for energy measurement. The sequence of states is simply encoded in Gray binary code during the synthesis process. This was considered as good idea for power reduction because the fact that the most states appear only once in 256-clock cycle lasting sequence. Beside, the state transition is regular in a way that for some state the next state is known in advance or there exist a small number of possible next states.

Decomposition of finite state machines has also been used to reduce the power.[8,9] The basic idea is to decompose the state transition graph of a finite state machine into two or more graphs that jointly produce the equivalent input-output behavior as the original machine. The states are partitioned by searching for a subset of states with high probability of transitions among these states and a low probability of transitions to and from other states. This subset of states then constitute a small sub-FSM which is active most of the time. When the small sub-FSM is active, the other larger sub-FSM can be disabled. Power is saved because, except for transitions between the two sub-FSMs, only one of the sub-FSMs needs to be clocked: the sub-FSM which is active at the moment. The other sub-FSMs which are not producing useful data are shut down by disabling the clock signal.

The non-optimized version of FSM (Block 5) has 4 input signals (beside clock and reset), 25 output signals, 229 states, and executes a state sequence which is periodically repeated with a period equal to 256 clock cycles. The FSM is decomposed into two sub FSMs: FSM1 and FSM2. The FSM1 controls the process of I^2, V^2, P and Q generation and accumulation, while, FSM2 is responsible for high-pass filtering and energy pulses generating. There exists only one transition from FSM1 to FSM2 during the main, 256 clock lasting period. The subsequences of states last 151 and 105 clock cycles for FSM1 and FSM2, respectivelly.

The additional control block determines which of two sub FSM is active at the moment. Each sub FSM generates a signal for ending of state sequence which is fed to the control block. The control block produces the two enable signals Enable1 and Enable2. When Enable1 signal is on for FSM1, it is off for FSM2. Conversely, the Enable2 signal is always off for FSM1 while it is on for FSM2.

Beside clock gating, the operand isolation technique is applied on finite state machines. To stop data propagation in the combinatorial logic block in inactive subFSM, the sequence of two-input AND cells are used in front of it. One of the inputs of AND cells is the FSM's input signal which is gated and the other one is the enable signal from control block.

The benefit in power reduction achieved by disabling a part of finite state machine is slighly degraded by new circuits introduced by decomposition. The new hardware consists of multiplexer circuits at the outputs of sub FSMs and adds extra switching activities.

The design in which the FSM is Gray encoded, and also incorporates clock gating, gives the power reduction of 35%. The final design where FSM is divided into two clock-gated sub-FSMs gives the minimal power consumption. Achieved consumption is 648μW and represents 42% reduction of consumption for non-optimized circuit

TABLE II

	FSM gray encoding		Decomposition with grey encoding	
Block	Area [gates]	Power [μW]	Area [gate]	Power [μW]
Clock tree	2	87	2	89
Registers	456	32	456	28
Three-state circuits	615	96	615	108
Adder	320	129	320	108
Multiplexer	307	41	307	30
Multiplier	663	94	663	94
FSM circuit	1081	258	1246	191
Total	3444	737	3609	648

III. Optimization of Embedded 8052 Microcontroller Block

A. *MCU's structure*

The instruction set of 8052 microcontroller (MCU) contains 255 instructions, which have variable length in range from one to three bytes. The opcode of an instruction is encoded in its first byte. The optional second and third bytes represent the operands. The instruction set can be considered as a complex, and, the 8052 microcontroller is classified as CISC (Complex Instruction Set Computer) [10,11]. The instructions can be divided into 5 main classes: arithmetical, logical, data transfer, boolean and jump instructions.

The complex and irregular instruction set increase the energy cost of fetching and decoding of instructions. Although the microcontroller does not represent the best choice for energy efficiency, the choice is justified by the fact that it is one of the most popular microcontrollers, which is often found in applications where the energy efficiency is important.

The global structure of microcontroller block embedded into Integrated Power Meter Chip consists of MCU core, memory blocks, the block for programming and initialization and peripheral units.

The MCU core performs fetching, decoding and executing of instructions and consists of Control logic block, Arithmetical-logical unit (ALU) and Special Function Registers I/O control logic.

The on-chip peripherals are comprised of: three digital input/output parallel ports (Port0 and Port1 are 8-bit and Port2 6-bit wide); LCD driver control circuit (driving up to 168 pixels LCD display) and several communication modules - two asynchronous universal receiver/transmitter blocks (USART0 and USART1) and one I2C-like serial interface. Also, three standard 8052 timer/counter circuits are present (TC0, TC1 and TC2).

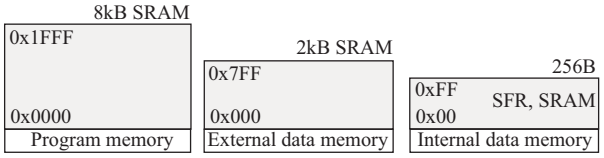

Fig.5. Microcontroller memories

The memory organization is similar to that of the industry standard 8052. Three main memory areas associated with the microcontroller are physically located on the Integrated Power Meter IC. They are illustrated in Fig. 5: Program memory (on-chip 8kB SRAM block), external data memory (physically consisting of XRAM - on-chip 2kB SRAM block, I/O RAM made of standard cells), and internal data memory (Internal RAM comprising of 256 Internal Dual port RAM and Special Function Registers).

The MCU doesn't have internal non-volatile memory for program storing. Instead, MCU utilize on-chip SRAM memory and external EEPROM chip. After the reset state, the program memory is automatically loaded from external EEPROM chip into 8kB SRAM block. The block for programming and initialization is responsible for this operation.

B. Optimization for low power

Optimization of microcontroller's power consumption is difficult task. Digital designers need to undertake a considerable amount of work to realize the most power efficient design.

The first implementation of MCU was made with two goals: to fulfil primary requirements concerning correct functioning, and the second, to use a minimal number of clock periods for an instruction execution. Since instruction set is complex (has 255 instructions), and 6 different addressing modes exist, the design of microcontroller demanded huge effort. The first implementation of microcontroller was made to be fully synchronous. The architecture has three pipeline stages that execute one-byte instructions in a single cycle. The activities within MCU core are localized as much as possible. Special function registers (SP, PSW, DTPR, A, B) are made to have their own data busses and function units (instead of using shared busses and units) for time saving.

When functionality was achieved, the power reduction became important issue. Clock gating schemes had been extensively used in the further MCU design. For low power consumption of increment logic a ripple carry adders were used. The result of power optimization of clock gating is given in Table III.

After clock gating, great effort was taken to minimize the switching activity: no register and execution unit receives control unless it processes data for a given instruction. Interrupts and pins only cause switching when accessed by software or when an input pin changes. Also, address and data lines for all memories have been made to change only when new data is to be read or written. The memories power save issue is particularly important because memories represent huge power consumers. In modern chips 30% of power is spent on read and write operations.

The total power reduction is 70% comparing the first implementation which met only functionality requirements.

C. MCU's Power saving modes

The implementation of power saving modes provides simple control of power consumption of microcontroller so the most appropriate operation mode can be chosen for any application. The MCU, beside Active operating mode, offers following low-power modes: Power Save, Standby and Power Down mode.

Power saving in Active operation mode should be explained first. One of the solutions to reduce power consumption in this mode is to reduce the clock frequency. Current consumption increases directly with the system clock frequency so keeping the system clock as low as possible is critical to keeping the power consumption down. In Active operation mode, few different clock frequencies are at disposal. The chip uses 32 kHz clock on-chip oscillator. Internal 4.1494 MHz clock signal is generated using on-chip PLL frequency multiplier and microcontroller has the option to use one of the outputs of clock divider circuit as the input clock signal. The nominal frequency of 4.194 MHz can be divided by one of the numbers 1, 2, 4, 8, 16, 32, 64 and 128. The user can select an optimal clock frequency instead of having highly power consuming microcontroller in a much slower system.

TABLE III

	Block	Non-optimized			Optimized by clock gating			Optimized by minimization of switching activity		
		Area [gates]	Power [µw]	Clk sinks	Area [gates]	Power [µw]	Clk sinks	Area [gates]	Power [µw]	Clk sinks
1.	Clock tree	0	5770	0	0	1420	0	0	642	0
2.	I/O RAM	2235	10	244	2174	21	23	2179	3	23
3.	DSP's interface	156	0	7	156	0	7	156	0	7
4.	Port0 circuit	328	26	16	328	14	16	314	27	16
5.	Port1 circuit	346	21	16	346	12	16	334	26	16
6.	Port2 circuit	188	20	12	188	13	12	186	27	12
7.	TC0 and TC1	968	58	57	754	43	21	755	55	21
8.	TC2	640	54	52	659	46	23	658	54	23
9.	UART 0	693	46	73	725	44	22	726	32	22
10.	UART 1	880	45	86	902	32	50	906	38	50
11.	I2C	597	41	21	597	33	21	593	44	21
12.	8052 core	4468	2010	266	3953	1990	104	4233	1286	104
13.	ALU	2331	452	120	2331	276	120	1965	200	120
14.	SFR read/write logic	992	97	84	941	82	38	986	140	38
15.	Programming and initialization logic	4675	163	428	4809	90	59		93	59
16.	LCD driver control	1081	33	1	1081	33	1	1091	28	1
		20578	8846	1483	19944	4149	533	15082	2695	533

The other power saving method used in Active operation mode is to gate the clock input of the microcontroller parts that are not used. The following peripheral units can be gated: Ports 0, 1, 2; Timer/Counters 0, 1, 2, UARTs 0, 1, and I2C communication controller.

The Power Save is very useful in applications in which microcontroller is often latently waiting the information from some sensor or other microcontroller. When the information is acquired, fast data processing is expected. In this mode, only clock input signal of the microcontroller is blocked out, peripheral units continue its normal operation. Like the Active operation mode, the selected peripheral units of the microcontroller can be gated. Disabling the peripheral modules results in 5-10% reduction of the total power consumption in Active mode, and 10-20% in Power Save mode.

The device can be turned back from Power Save mode to the Active operation mode by two different events: the system reset and interrupt. In the case of interrupt request, the MCU continues with the execution of the next program command and after that starts processing the interrupt and jumping to the interrupt processing routine. The MCU's wake up by reset restarts the program execution. Since the clock generator is active in this mode the wake-up time is short.

In Standby mode, the clock generator producing main clock is operative but clock inputs of microcontroller and peripheral units are gated. In Power Down mode, everything is shut down including the main clock source.

The clock controller module is the part of microcontroller block responsible for power saving modes. The module produces two main clock signals, one dedicated to microcontroller and the other one clocking the peripheral units. During the Active operation both signals behave equally. In low–power operation modes one or both of the clock signals are stopped. Low-power modes are simply invoked by writing to one of the Special Function registers dedicated for power management.

IV. THE OPTIMIZATION FOR LOW-POWER OF IPM'S DIGITAL BLOCKS

TABLE IV

Block	Area [gates]	Power [mW]
Sinc- Current	4623	0.238
Sinc- Voltage	7077	0.275
FIR - Current	6491	0.472
FIR- Voltage	6607	0.489
Hilbert filter	8820	0.323
DSP	21425	1.150
RTC	1437	0.002
XRAM - 2kB	18884	0.010
Int. Dual Port RAM – 256B	7796	0.310
Program memory SRAM 8kB	50030	2.238
MCU	15082	2.695
Total:	148272	8.202

The power optimization results for digital blocks are obtained after Verilog simulations during which complete switching activity was recorded.

The chip was implemented in AMI CMOS 0.35µm standard cell technology. Design was first described in VHDL, and after, synthesized by Cadence's Build Gates tool. The digital signal blocks of Integrated Power Meter

are carefully designed to prevent synchronization errors between them. Also, the blocks are power optimized using techniques described above. The layout was generated by Cadence's tool First Encounter. Signal delays were obtained considering parasitic capacitances of nets in the layout. The Verilog netlists, extracted from layout, were simulated by NCSim logical verification tool. Switching activity file, which was obtained after Verilog simulation, was imported into First Encounter for estimation of average power consumption.

The power consumption of blocks is given in the Table I. Two blocks that consume the most of power are MCU and DSP block. The total power consumption of digital part of a chip is 8.202mW.

IV. CONCLUSION

In this paper, a low power Integrated Power Meter IC is presented. The chip incorporates several digital data processing blocks: filters, digital signal processor dedicated to power metering and embedded microcontroller.

Two blocks identified as blocks with the highest power consumption are DSP block and embedded microcontroller. The applied low-power techniques are mainly based on clock and data gating. Clock gating incorporated into the DSP induced the significant power saving - reducing the overall power by 27%. After DSP's state machine had been Gray encoded, the power reduction gain became 35%. The total power reduction of 42% is achieved by FSM's state decomposition used along with the other two techniques.

Great effort was taken to minimize the switching activity of embedded MCU: no register and execution unit receives control unless it processes data for a given instruction. The microcontroller's control logic was built in a way that address and data lines for the memories change only when new data is to be read or written. The clock gating was used in the design wherever it was possible. The total power reduction is 70% comparing the first implementation which met only functionality requirements.

The main objective, which was to realize power efficient design, was fully reached. Measurement on the chip, which will be in manufacture, has to be carried out, to confirm those results.

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